Enhanced Hole Mobilities in Surface-channel Strained-Si *p*-MOSFETs

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Abstract

The strain dependence of the hole mobility in surface-channel *p*-MOSFETs employing pseudomorphic, strained-Si layers is reported for the first time. The hole mobility enhancement is observed to increase roughly linearly with the strain as the Ge content in the relaxed $Si_{1-x}Ge_x$ buffer layer increases. When compared to the device with $x = 0.1$, the devices with $x = 0.22$ and 0.29 exhibit hole mobility enhancement factors of 1.4 and 1.8, respectively. In spite of the high fixed charge in our gate oxides, the device with Ge content $x = 0.29$ still exhibits a mobility 1.3 times that of bulk Si MOSFETs with state-of-the-art oxides. The first measurements of the transconductance enhancements in sub-micron strained-Si *p*-MOSFETs are also reported.

Introduction

Performance enhancements have previously been demonstrated in *n*-MOSFETs employing pseudomorphic, strained-Si channels [1]. The room temperature electron mobility enhancement saturates at about 1.8 for Ge contents $x > 0.2$. Strained-Si *p*-MOSFETs, which are desirable for CMOS applications, have also been reported [2], but quantitative analysis of the mobility enhancement has been hindered by carrier confinement in the parasitic, buried $Si_{1-x}Ge_x$ layer. In this work, a modified layer structure which eliminates this problem was used.

In bulk Si, the heavy- and light-hole bands are degenerate at the Γ point. The biaxial tension in strained-Si layers grown on relaxed $Si_{1-x}Ge_x$ lifts the degeneracy, splitting these bands [3]. The strain also lowers the spin-orbit band and deforms all the bands, changing the hole effective mass in each. The hole mobility is thus enhanced by decreased inter-band scattering and reduced in-plane effective mass. In this work, long channel *p*-MOSFETs are analyzed to characterize the behavior of the hole mobility as a function of strain in the Si channel.

Device Structure

Epitaxial layers were grown at 750 and 700°C by chemical vapor deposition. *p*-MOSFETs with *in-situ* doped n^+ polysilicon gates were fabricated using the process described in [4]. Wet thermal oxidation (750°C) of the strained-Si layer at the surface was used to form a 13 nm-thick gate oxide. Fig. 1 shows the basic device structure. The final Ge content of the relaxed buffer layers was varied from $x = 0.1$ to 0.29 to vary the strain in the Si channel. The epitaxial layers were *in-situ* doped with As (6×10^{16} to 2×10^{17} cm^{-3}). Epitaxial Si wafers, which were inadvertently doped more lightly (3 ~ 4 times), and a Czochralski (CZ) Si wafer, were processed along with the strained-Si wafers to act as controls. After device processing, Rutherford back-scattering (RBS) and Raman spectroscopy were used to measure the Ge compositions, thicknesses, and strain state of the layers, verifying that the Si layers remain pseudomorphic to the relaxed $Si_{1-x}Ge_x$ buffer layers.

To avoid confining holes in the relaxed $Si_{1-x}Ge_x$, a grade-back layer ($Si_{1-y}Ge_y$) was inserted just below the strained-Si channel. Fig. 2 shows calculated energy band diagrams with and without this grade-back layer. In a structure without a grade-back layer, the discontinuity in the valence band confines the holes and forms a parasitic buried channel (Fig. 2(a)). The mobility in this relaxed $Si_{1-x}Ge_x$ channel is expected to be low [5], and the increased separation between the gate and the buried channel will degrade the transconductance g_m. Hence, in such devices, the performance enhancement will be limited, especially at low gate overdrive $|V_g-V_t|$ as observed in [2].

The strained, graded $Si_{1-y}Ge_y$ layer just below the surface strained-Si layer reduces the band discontinuity (Fig. 2(b)). As shown by the calculations in Fig. 3, the reduction of the valence band discontinuity by the grade-back layer significantly reduces the hole concentration in the underlying, parasitic $Si_{1-x}Ge_x$ channel. Even at low gate bias, the hole concentration is approximately two orders of magnitude larger in the Si surface channel than in the underlying layers. Thus, for the entire gate bias range, the drain current will be dominated by hole transport in the strained-Si, preserving the advantages of a surface channel device and allowing direct measurement of the strained-Si hole mobility.

Electrical Characterization

The gate-channel (C_{gc}) and gate-bulk (C_{gb}) capacitances were determined by split *C-V* measurements on the MOSFETs [6]. Fig. 4 illustrates a measured *C-V* profile for a strained-Si device and the simulated capacitance curve [7], which was used to extract the doping profile and the fixed charge.

Fig. 5 shows the output characteristics for a strained-Si device with $x = 0.29$ and $L_{eff} = 50$ μm. The curves exhibit

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well-behaved long channel MOSFET characteristics. Larger devices (200 × 100 μm) were used to extract the effective hole mobility, $\mu_{eff} = (\partial I/\partial V_{DS})\cdot(L/W)/Q_{inv}$ as a function of vertical effective electric field, $E_{eff} = \frac{1}{\varepsilon_{Si}}(Q_b + \frac{1}{\eta}Q_{inv})$ where η is taken to be 3 for holes [8]. The inversion charge Q_{inv} was found by integrating C_{gc} from the split C-V measurements, and the bulk charge Q_b was calculated by integrating the extracted doping profile in the depletion region.

Fig. 6 shows μ_{eff} as a function of E_{eff} at 295K for strained-Si p-MOSFETs with final Ge contents x = 0.10, 0.22, and 0.29 in the relaxed buffer layers. Note that μ_{eff} increases with strain over the entire range of E_{eff}. The peak mobility of each sample is shown as a function of doping and strain in Fig. 7. When compared to the device with $x = 0.10$, the devices with x = 0.22 and 0.29 exhibit peak mobility enhancement ratios of 1.4 and 1.8, respectively, indicating an approximately linear rise in mobility with strain. The epitaxial layer doping decreases towards the surface, and the horizontal error bars in Fig. 7 represent the doping range in the near-surface region.

To roughly account for the unintentional doping differences between the MOSFETs, we utilize the dependence of μ_{eff} on doping for state-of-the-art Si devices (Fig. 7, dashed line) [9]. We assume that the mobility of all our devices is degraded by the high oxide fixed charge (~4 × 10^{11} cm^{-2}). Mathiessen's rule is used to extract the magnitude of the oxide-fixed-charge-mobility:

$$\mu_{(q_f)} = \{1/\mu_{(meas.)} - 1/\mu_{(state\text{-}of\text{-}the\text{-}art)}\}^{-1}$$

where $\mu_{(meas.)}$ represents the measured mobility for our unstrained-Si control devices. We find that $\mu_{(q_f)} \cong 700\ cm^2/V\cdot sec$. Assuming that $\mu_{(q_f)}$ is independent of doping, the expected unstrained Si mobility is given by:

$$\mu(N_d)_{(Si\ adjusted)} = \{1/\mu(N_d)_{(state\text{-}of\text{-}the\text{-}art)} - 1/\mu_{(q_f)}\}^{-1}$$

These values are shown by the solid line in Fig. 7. The observed increase in μ_{eff} with strain is far greater than the enhancement expected from the variation in channel doping between samples.

Using this extrapolation, when the hole mobility in the strained-Si device with x = 0.29 is compared to the expected mobility for an unstrained Si device with comparable doping and Q_f, the maximum mobility enhancement factor is 1.7. When compared directly to the peak mobility values of [9] for p-MOSFETs with state of the art oxides, the hole mobility is still enhanced by a factor of 1.2 to 1.3.

The performance of short channel devices also improves with strain. Fig. 8 shows the transconductance g_m for devices with L_{eff} of 0.5 μm.

Comparison with Strained-Si *n*-MOSFETs

At room temperature, the mobility enhancement ratio for electrons saturates at approximately 1.8 for $x > 0.2$ [1, 10]. For the p-MOSFETs studied in this work, the mobility enhancement does not saturate, in agreement with theoretical calculations for the bulk strained-Si hole mobility [11]. The difference between the strain dependence of the electron and hole mobilities may be partially explained by the different energy splitting at the band minima. For x = 0.2, the valence band splitting is 77 meV [11], compared to 134 meV for the conduction band splitting. The electron mobility enhancement saturates with increasing strain because eventually, inter-band scattering is significantly suppressed, so that other scattering mechanisms dominate. Hence, further band splitting results in negligible mobility increase. The smaller valence band splitting for a given strain suggests that mobility saturation, if it does occur, will take place at higher strains for holes than for electrons. In addition, the observed hole mobility may not saturate because the valence band continues to deform with increasing strain, while the conduction band effective masses remain essentially unchanged [10].

Summary

The first measurements of the strain dependence of the hole mobility in surface-channel, strained-Si p-MOSFETs are reported. The measured hole mobility increases roughly linearly with strain, in agreement with published calculations. Devices with Ge contents x = 0.29 exhibit peak hole mobility enhancement factors of 1.8, compared to devices with x = 0.1. The transconductance in sub-micron devices also increases with strain. In contrast to strained-Si n-MOSFETs, the mobility enhancement for the p-MOSFETs does not saturate for $x < 0.3$, suggesting that further improvements in p-MOSFETs may be possible by increasing the strain in the Si channel. These results imply that a single epitaxial layer structure could be used for the fabrication of both n- and p-MOS *surface channel* FETs, which would be attractive for enhanced CMOS applications.

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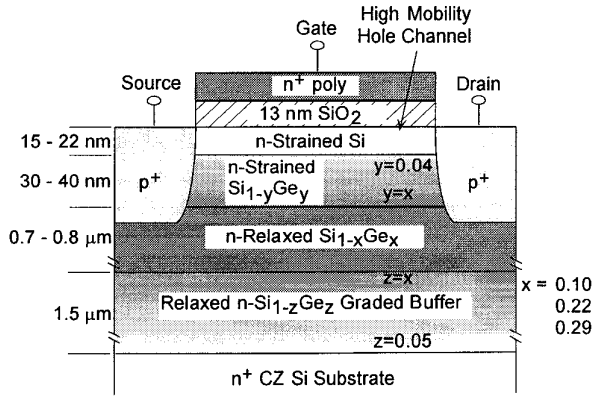

Fig. 1 Basic structure of strained Si *p*-MOSFET with a graded Si-channel/$Si_{1-y}Ge_y$ interface.

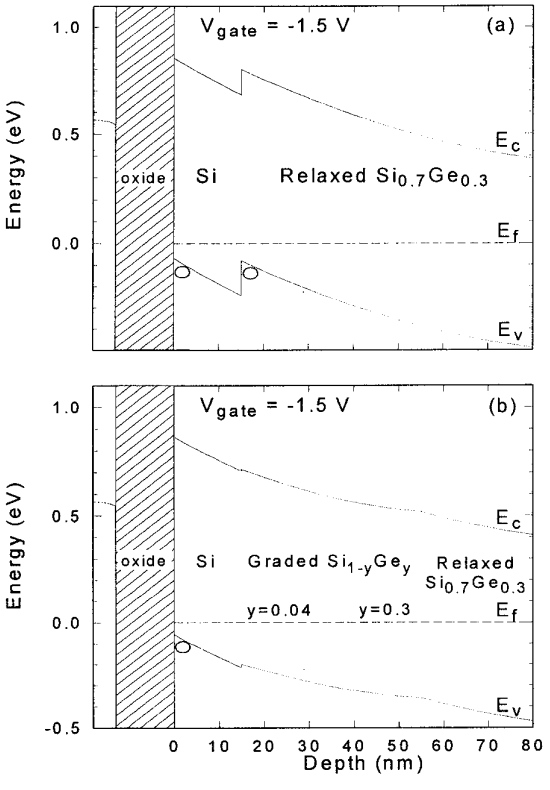

Fig. 2 Calculated energy band diagrams for an (a) abrupt and a (b) graded Si-channel/$Si_{1-y}Ge_y$ interface. Note the absence of a parasitic, buried channel in the graded interface structure (b).

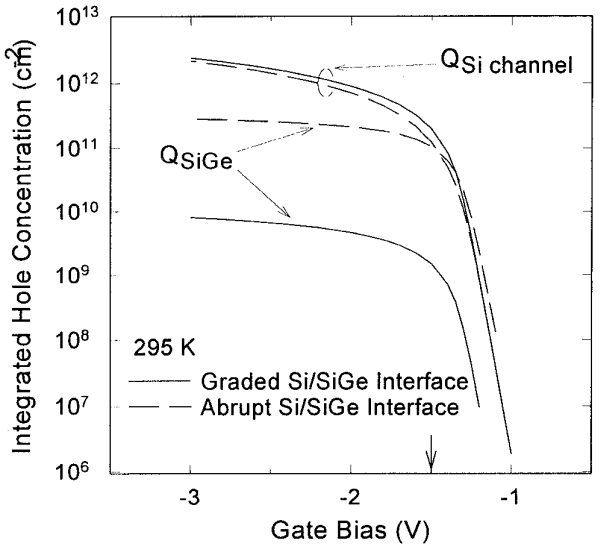

Fig. 3 Calculated hole concentration in surface and buried channels for the structures in Fig. 2. The arrow indicates the gate bias for the calculation in Fig. 2.

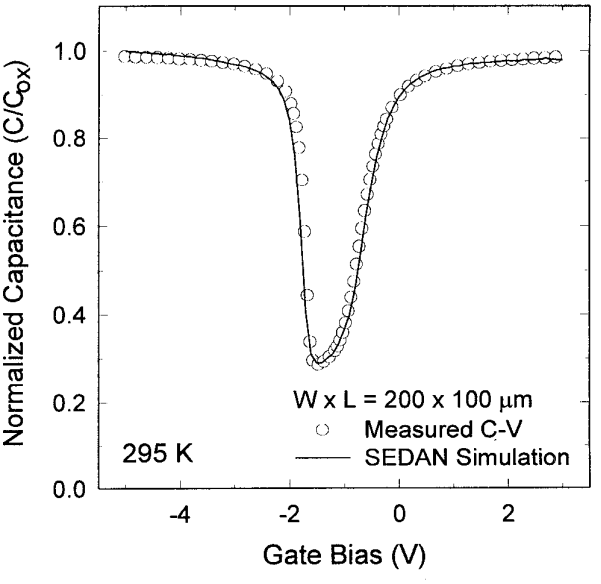

Fig. 4 Measured and simulated *C-V* profile (40 kHz) for a strained-Si device on a 29% Ge buffer layer. The *C-V* curve is obtained by adding C_{gc} and C_{gb} from split *C-V* measurement.

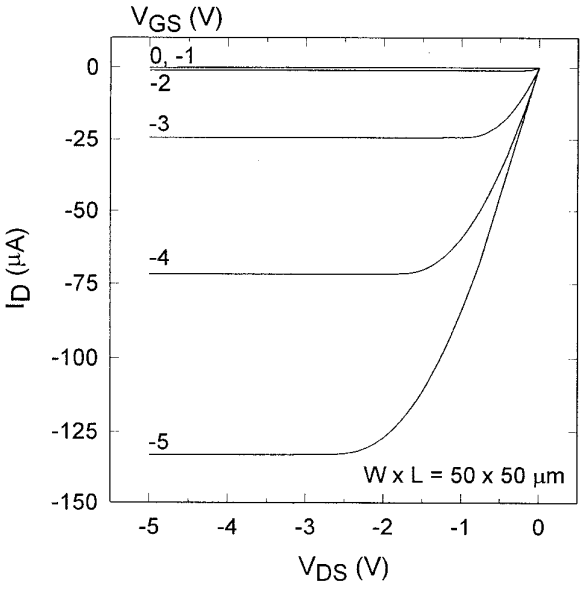

Fig. 5 Output characteristics for a large-area strained-Si device on a 29% Ge buffer layer.

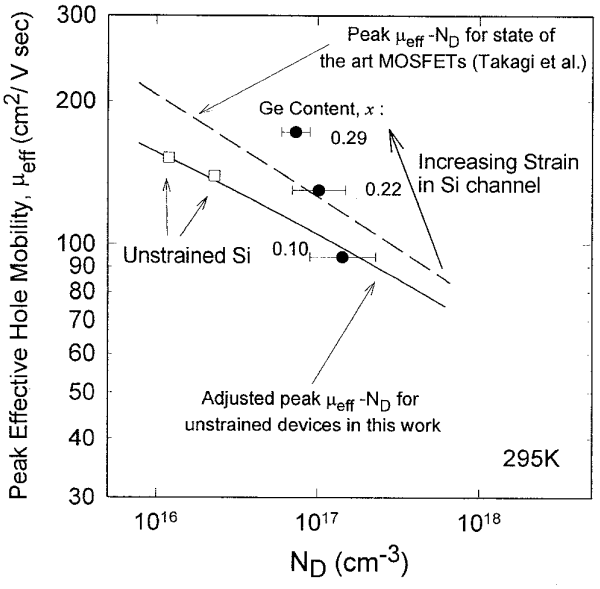

Fig.7 Peak effective mobility versus doping at V_{DS}= -10mV for strained and unstrained transistors. Note the strain increases as x increases from 0.10 to 0.29.

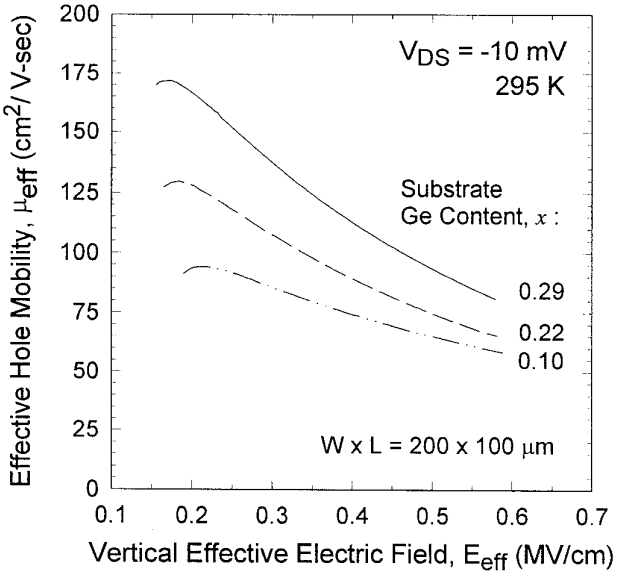

Fig. 6 Measured effective mobility versus effective electric field for long channel strained-Si devices at room temperature.

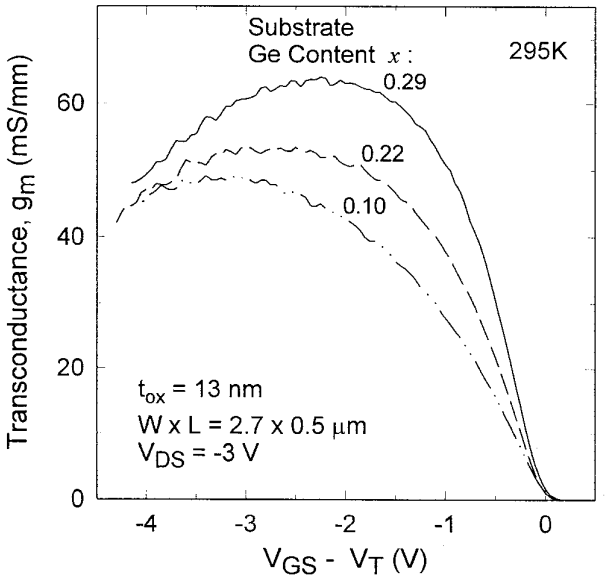

Fig. 8 Short channel device transconductance g_m for the strained-Si p-MOSFETs.